High Speed, ESD-Protected, Half-/Full-Duplex *i*Coupler Isolated RS-485 Transceiver

ADM2491E

FEATURES

- Isolated, RS-485/RS-422 transceiver, configurable as half- or full-duplex
- ±8 kV ESD protection on RS-485 input/output pins
- 16 Mbps data rate
- Complies with ANSI TIA/EIA RS-485-A-1998 and ISO 8482: 1987(E)
- Suitable for 5 V or 3.3 V operation (V_{DD1})
- High common-mode transient immunity: >25 kV/μs
- Receiver has open-circuit, fail-safe design
- 32 nodes on the bus
- Thermal shutdown protection
- Safety and regulatory approvals
  - UL recognition: 5000 V rms isolation voltage for 1 minute, per UL 1577
  - VDE certificate of conformity
    - DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12
    - Reinforced insulation, V_{IORM} = 848 V peak
- Operating temperature range: −40°C to +85°C
- Wide body, 16-lead SOIC package

APPLICATIONS

- Isolated RS-485/RS-422 interfaces
- Industrial field networks
- INTERBUS
- Multipoint data transmission systems

FUNCTIONAL BLOCK DIAGRAM

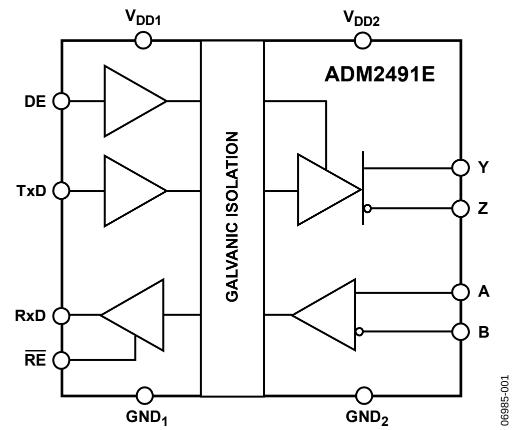

Figure 1.

GENERAL DESCRIPTION

The ADM2491E is an isolated data transceiver with ±8 kV ESD protection and is suitable for high speed, half- or full-duplex communication on multipoint transmission lines. For half-duplex operation, the transmitter outputs and the receiver inputs share the same transmission line. Transmitter output Pin Y is linked externally to receiver input Pin A, and transmitter output Pin Z is linked to receiver input Pin B.

The ADM2491E is designed for balanced transmission lines and complies with ANSI TIA/EIA RS-485-A-1998 and ISO 8482: 1987(E). The device employs Analog Devices, Inc., *i*Coupler® technology to combine a 3-channel isolator, a three-state differential line driver, and a differential input receiver into a single package.

The differential transmitter outputs and receiver inputs feature electrostatic discharge circuitry that provides protection to ±8 kV using the human body model (HBM). The logic side of the device can be powered with either a 5 V or a 3.3 V supply, whereas the bus side requires an isolated 5 V supply.

The device has current-limiting and thermal shutdown features to protect against output short circuits and situations in which bus contention could cause excessive power dissipation.

The ADM2491E is available in a wide body, 16-lead SOIC package and operates over the −40°C to +85°C temperature range.

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REVISION HISTORY

12/08—Rev. 0 to Rev. A

Updated Regulatory Approval Status Throughout ... 1
Changes to Table 7 ... 6

10/07—Revision 0: Initial Version

SPECIFICATIONS

All voltages are relative to their respective ground; 3.0 V ≤ V_{DD1} ≤ 5.5 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V. All minimum/maximum specifications apply over the entire recommended operation range, unless otherwise noted. All typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 5.0 V, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
SUPPLY CURRENT						
Power Supply Current, Logic Side						
TxD/RxD Data Rate = 2 Mbps	I_{DD1}			3.0	mA	Unloaded output
TxD/RxD Data Rate = 16 Mbps	I_{DD1}			6	mA	Half-duplex configuration, $R_{TERMINATION}$ = 120 Ω, see Figure 5
Power Supply Current, Bus Side						
TxD/RxD Data Rate = 2 Mbps	I_{DD2}			4.0	mA	Unloaded output
TxD/RxD Data Rate = 16 Mbps	I_{DD2}			50	mA	V_{DD2} = 5.5 V, half-duplex configuration, $R_{TERMINATION}$ = 120 Ω, see Figure 5
DRIVER						
Differential Outputs						
Differential Output Voltage, Loaded	$\lvert V_{OD}\rvert$	2.0		5.0	V	R_L = 100 Ω (RS-422), see Figure 3
		1.5		5.0	V	R_L = 54 Ω (RS-485), see Figure 3
		1.5		5.0	V	−7 V ≤ V_{TEST1} ≤ 12 V, see Figure 4
Δ$\lvert V_{OD}\rvert$ for Complementary Output States	Δ$\lvert V_{OD}\rvert$			0.2	V	R_L = 54 Ω or 100 Ω, see Figure 3
Common-Mode Output Voltage	V_{OC}			3.0	V	R_L = 54 Ω or 100 Ω, see Figure 3
Δ$\lvert V_{OC}\rvert$ for Complementary Output States	Δ$\lvert V_{OC}\rvert$			0.2	V	R_L = 54 Ω or 100 Ω, see Figure 3
Output Leakage Current (Y, Z)	I_O			100	µA	DE = 0 V, V_{DD2} = 0 V or 5 V, V_{IN} = 12 V
		−100			µA	DE = 0 V, V_{DD2} = 0 V or 5 V, V_{IN} = −7 V
Short-Circuit Output Current	I_{OS}			250	mA	
Logic Inputs DE, $\overline{RE}$, TxD						
Input Threshold Low	V_{IL}	0.25 × V_{DD1}			V	
Input Threshold High	V_{IH}			0.7 × V_{DD1}	V	
Input Current	I_{TxD}	−10	+0.01	+10	µA	
RECEIVER						
Differential Inputs						
Differential Input Threshold Voltage	V_{TH}	−0.2		+0.2	V	
Input Voltage Hysteresis	V_{HYS}		30		mV	V_{OC} = 0 V
Input Current (A, B)	I_I			+1.0	mA	V_{OC} = 12 V
		−0.8			mA	V_{OC} = −7 V
Line Input Resistance	R_{IN}	12			kΩ	
Logic Outputs						
Output Voltage Low	V_{OLRxD}		0.2	0.4	V	I_{ORxD} = 1.5 mA, V_A − V_B = −0.2 V
Output Voltage High	V_{OHRxD}	V_{DD1} − 0.3	V_{DD1} − 0.2		V	I_{ORxD} = −1.5 mA, V_A − V_B = 0.2 V
Short-Circuit Current				100	mA	
Three-State Output Leakage Current	I_{OZR}			±1	µA	V_{DD1} = 5.5 V, 0 V < V_{OUT} < V_{DD1}
COMMON-MODE TRANSIENT IMMUNITY[1]		25			kV/µs	V_{CM} = 1 kV, transient magnitude = 800 V

[1] CM is the maximum common-mode voltage slew rate that can be sustained while maintaining specification-compliant operation. V_{CM} is the common-mode potential difference between the logic and bus sides. The transient magnitude is the range over which the common mode is slewed. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

TIMING SPECIFICATIONS

T_A = −40°C to +85°C.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DRIVER						
Maximum Data Rate		16			Mbps	
Propagation Delay	t_{PLH}, t_{PHL}		45	60	ns	R_L = 54 Ω, C_{L1} = C_{L2} = 100 pF, see Figure 6 and Figure 10
Pulse Width Distortion, $t_{PWD} = \|t_{PYLH} - t_{PYHL}\|$, $t_{PWD} = \|t_{PZLH} - t_{PZHL}\|$	t_{PWD}			7	ns	R_L = 54 Ω, C_{L1} = C_{L2} = 100 pF, see Figure 6 and Figure 10
Single-Ended Output Rise/Fall Times	t_R, t_F			20	ns	R_L = 54 Ω, C_{L1} = C_{L2} = 100 pF, see Figure 6 and Figure 10
Enable Time				55	ns	R_L = 110 Ω, C_L = 50 pF, see Figure 8 and Figure 11
Disable Time				55	ns	R_L = 110 Ω, C_L = 50 pF, see Figure 8 and Figure 11
RECEIVER						
Propagation Delay	t_{PLH}, t_{PHL}			60	ns	C_L = 15 pF, see Figure 7 and Figure 12
Pulse Width Distortion, $t_{PWD} = \|t_{PLH} - t_{PHL}\|$	t_{PWD}			10	ns	C_L = 15 pF, see Figure 7 and Figure 12
Enable Time				13	ns	R_L = 1 kΩ, C_L = 15 pF, see Figure 9 and Figure 13
Disable Time				13	ns	R_L = 1 kΩ, C_L = 15 pF, see Figure 9 and Figure 13

PACKAGE CHARACTERISTICS

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Resistance (Input to Output)[1]	R_{I-O}		10^{12}		Ω	
Capacitance (Input to Output)[1]	C_{I-O}		3		pF	f = 1 MHz
Input Capacitance[2]	C_I		4		pF	
Input IC Junction-to-Case Thermal Resistance	θ_{JCI}		33		°C/W	Thermocouple located at center of package underside
Output IC Junction-to-Case Thermal Resistance	θ_{JCO}		28		°C/W	

[1] Device considered a 2-terminal device: Pin 1, Pin 2, Pin 3, Pin 4, Pin 5, Pin 6, Pin 7, and Pin 8 are shorted together, and Pin 9, Pin 10, Pin 11, Pin 12, Pin 13, Pin 14, Pin 15, and Pin 16 are shorted together.
[2] Input capacitance is from any input data pin to ground.

REGULATORY INFORMATION

Table 4.

UL[1]	VDE[2]
Recognized under the 1577 component recognition program[1]	Certified according to DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12[2]
5000 V rms isolation voltage	Reinforced insulation, 846 V peak

[1] In accordance with UL 1577, each ADM2491E is proof tested by applying an insulation test voltage ≥ 6000 V rms for 1 second (current leakage detection limit = 10 μA).
[2] In accordance with DIN V VDE V 0884-10, each ADM2491E is proof tested by applying an insulation test voltage ≥ 1590 V peak for 1 second (partial discharge detection limit = 5 pC).

INSULATION AND SAFETY-RELATED SPECIFICATIONS

Table 5.

Parameter	Symbol	Value	Unit	Conditions
Rated Dielectric Insulation Voltage		5000	V rms	1 minute duration
Minimum External Air Gap (Clearance)	L(I01)	7.7	mm min	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L(I02)	8.1	mm min	Measured from input terminals to output terminals, shortest distance along body
Minimum Internal Gap (Internal Clearance)		0.017	mm min	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89)

VDE 0884 INSULATION CHARACTERISTICS

This isolator is suitable for basic electrical isolation only within the safety limit data. Maintenance of the safety data must be ensured by means of protective circuits.

An asterisk (*) on a package denotes VDE 0884 approval for 848 V peak working voltage.

Table 6.

Description	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110 for Rated Mains Voltage			
≤300 V rms		I to IV	
≤450 V rms		I to II	
≤600 V rms		I to II	
Climatic Classification		40/105/21	
Pollution Degree (DIN VDE 0110, see Table 1)		2	
Maximum Working Insulation Voltage	V_{IORM}	846	V peak
Input-to-Output Test Voltage, Method b1	V_{PR}	1590	V peak
$V_{IORM} \times 1.875 = V_{PR}$, 100% Production Tested, $t_m = 1$ sec, Partial Discharge < 5 pC			
Input-to-Output Test Voltage, Method a	V_{PR}		
After Environmental Tests, Subgroup 1		1357	V peak
$V_{IORM} \times 1.6 = V_{PR}$, $t_m = 60$ sec, Partial Discharge < 5 pC			
After Input and/or Safety Test, Subgroup 2/Subgroup 3		1018	V peak
$V_{IORM} \times 1.2 = V_{PR}$, $t_m = 60$ sec, Partial Discharge < 5 pC			
Highest Allowable Overvoltage (Transient Overvoltage, $t_{TR} = 10$ sec)	V_{TR}	6000	V peak
Safety-Limiting Values (Maximum Value Allowed in the Event of a Failure, see Figure 20)			
Case Temperature	T_S	150	°C
Input Current	$I_{S, INPUT}$	265	mA
Output Current	$I_{S, OUTPUT}$	335	mA
Insulation Resistance at T_S, $V_{IO} = 500$ V	R_S	$>10^9$	Ω

ABSOLUTE MAXIMUM RATINGS

T_A = 25 °C, unless otherwise noted. Each voltage is relative to its respective ground.

Table 7.

Parameter	Rating
Storage Temperature	−55°C to +150°C
Ambient Operating Temperature	−40°C to +85°C
V_{DD1}	−0.5 V to +7 V
V_{DD2}	−0.5 V to +6 V
Logic Input Voltages	−0.5 V to V_{DD1} + 0.5 V
Bus Terminal Voltages	−9 V to +14 V
Logic Output Voltages	−0.5 V to V_{DD1} + 0.5 V
Average Output Current, per Pin	±35 mA
ESD (Human Body Model) on A, B, Y, and Z Pins	±8 kV
θ_{JA} Thermal Impedance	60°C/W

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Absolute maximum ratings apply individually only, not in combination.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTIONAL DESCRIPTIONS

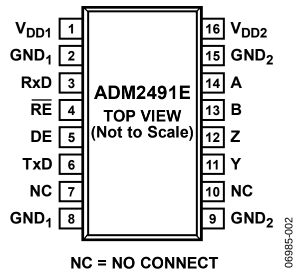

Figure 2. ADM2491E Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	Power Supply (Logic Side). Decoupling capacitor to GND_1 required; capacitor value should be between 0.01 µF and 0.1 µF.
2, 8	GND_1	Ground (Logic Side).
3	RxD	Receiver Output.
4	$\overline{RE}$	Receiver Enable Input. Active low logic input. When this pin is low, the receiver is enabled; when high, the receiver is disabled.
5	DE	Driver Enable Input. Active high logic input. When this pin is high, the driver (transmitter) is enabled; when low, the driver is disabled.
6	TxD	Transmit Data.
7, 10	NC	No Connect. This pin must be left floating.
9, 15	GND_2	Ground (Bus Side).
11	Y	Driver Noninverting Output.
12	Z	Driver Inverting Output.
13	B	Receiver Inverting Input.
14	A	Receiver Noninverting Input.
16	V_{DD2}	Power Supply (Bus Side). Decoupling capacitor to GND_2 is required; capacitor value should be between 0.01 µF and 0.1 µF.

TEST CIRCUITS

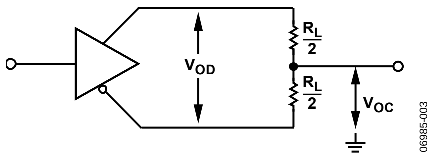

Figure 3. Driver Voltage Measurement

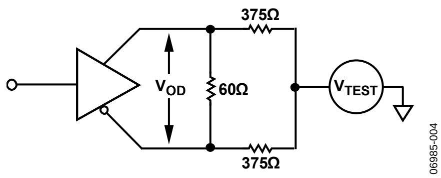

Figure 4. Driver Voltage Measurement

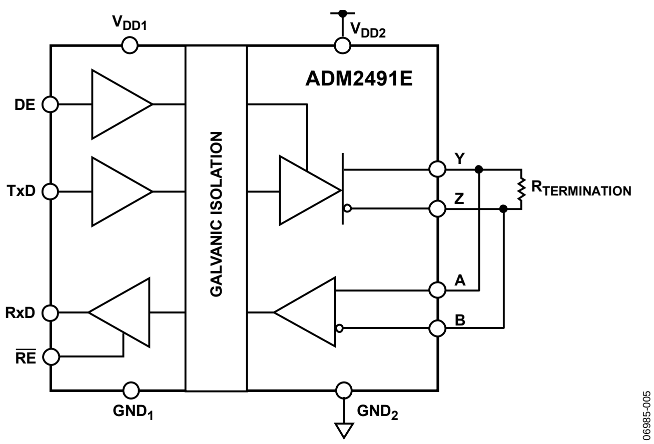

Figure 5. Supply Current Measurement Test Circuit

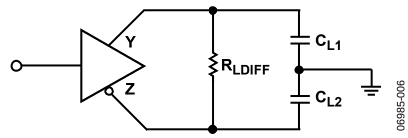

Figure 6. Driver Propagation Delay

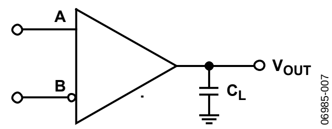

Figure 7. Receiver Propagation Delay

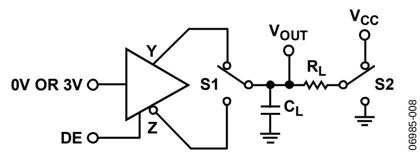

Figure 8. Driver Enable/Disable

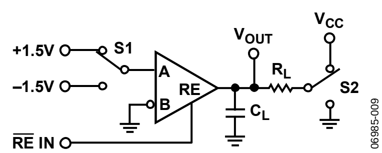

Figure 9. Receiver Enable/Disable

SWITCHING CHARACTERISTICS

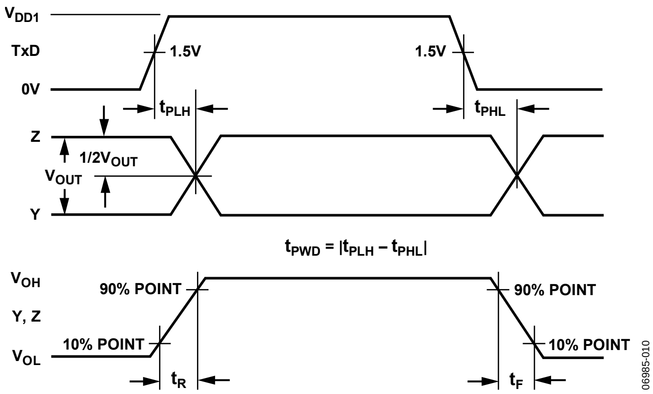

Figure 10. Driver Propagation Delay, Rise/Fall Timing

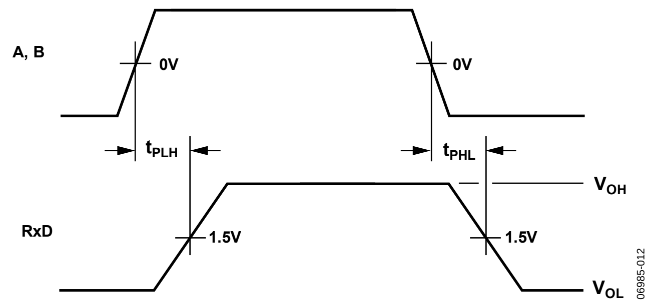

Figure 12. Receiver Propagation Delay

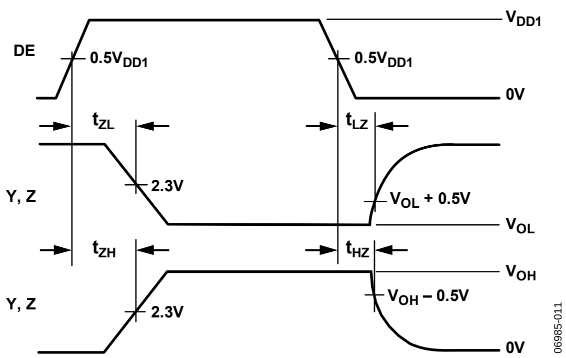

Figure 11. Driver Enable/Disable Delay

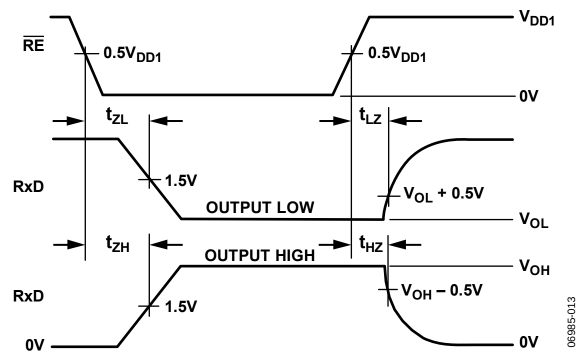

Figure 13. Receiver Enable/Disable Delay

TYPICAL PERFORMANCE CHARACTERISTICS

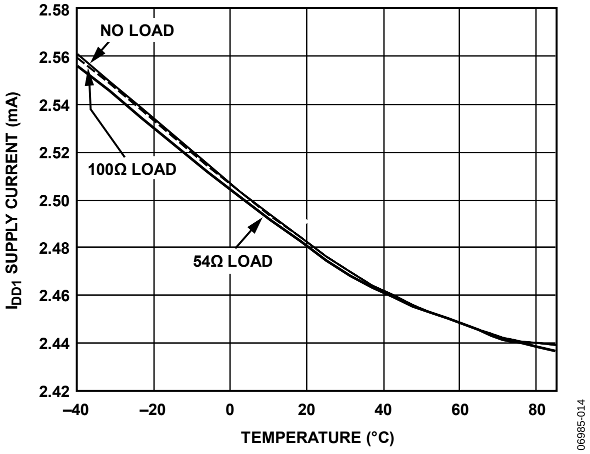

Figure 14. I_{DD1} Supply Current vs. Temperature

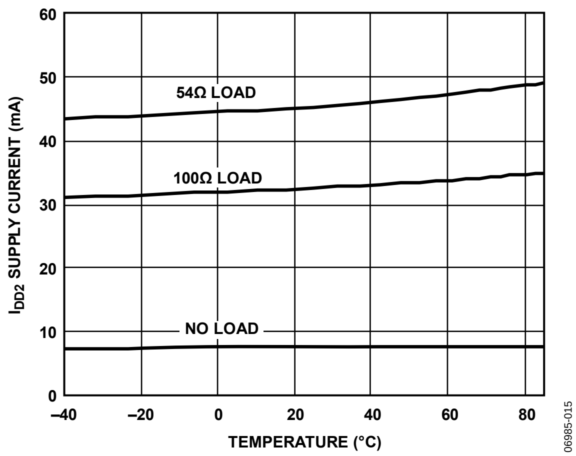

Figure 15. I_{DD2} Supply Current vs. Temperature

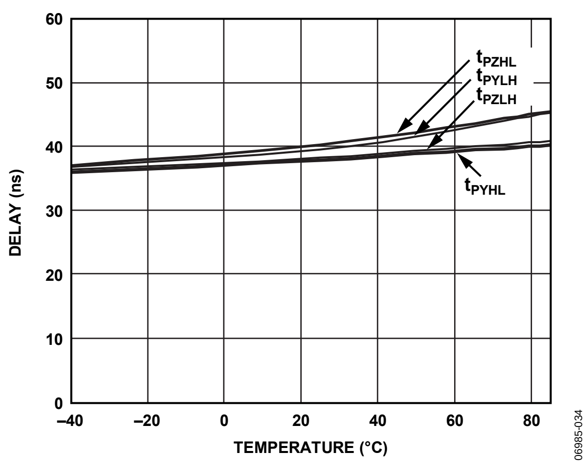

Figure 16. Driver Propagation Delay vs. Temperature

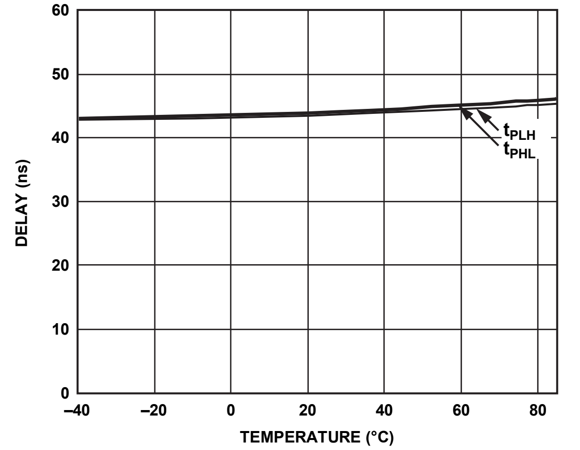

Figure 17. Receiver Propagation Delay vs. Temperature

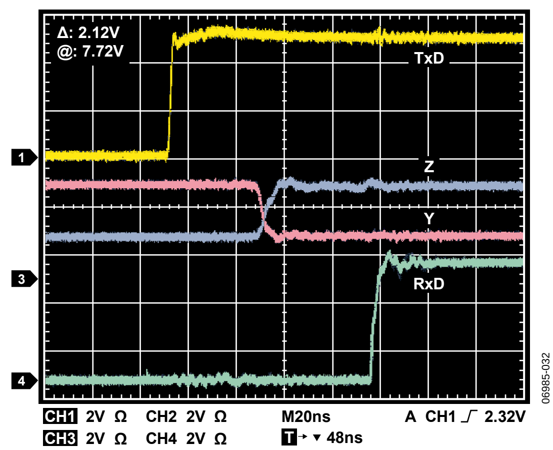

Figure 18. Driver/Receiver Propagation Delay, Low to High (R_{LDIFF} = 54 Ω, C_{L1} = C_{L2} = 100 pF)

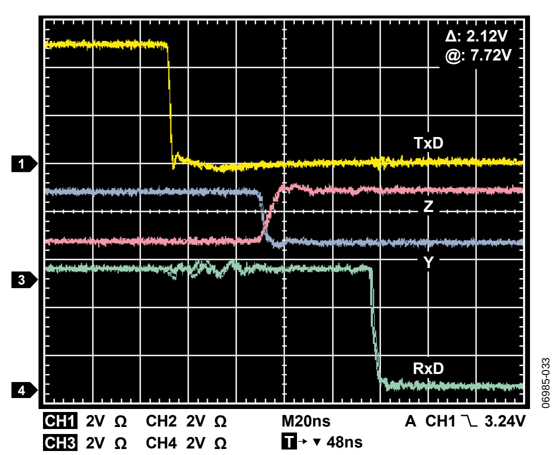

Figure 19. Driver/Receiver Propagation Delay, High to Low (R_{LDIFF} = 54 Ω, C_{L1} = C_{L2} = 100 pF)

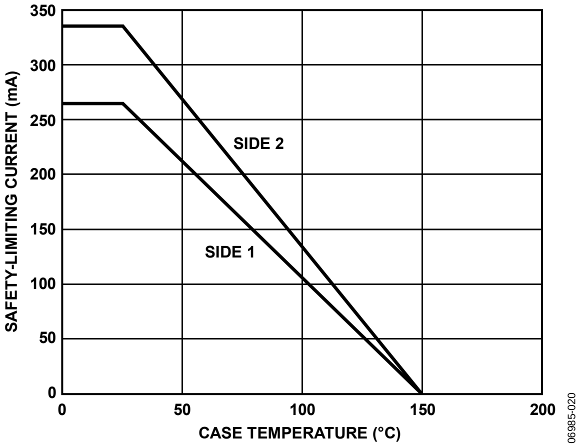

Figure 20. Thermal Derating Curve, Dependence of Safety-Limiting Values with Case Temperature per VDE 0884

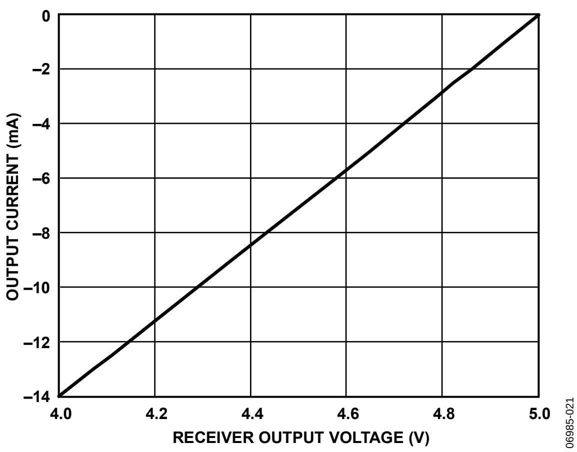

Figure 21. Output Current vs. Receiver Output High Voltage

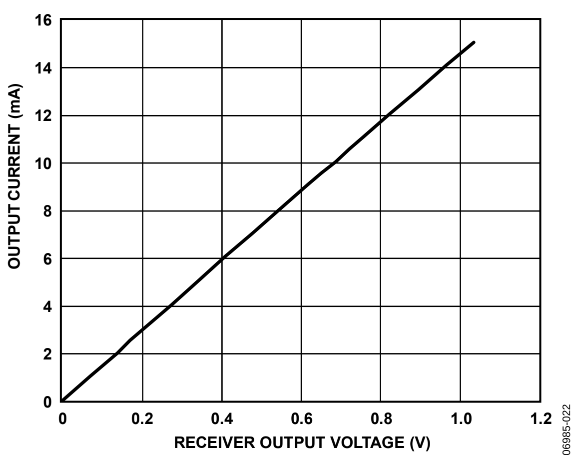

Figure 22. Output Current vs. Receiver Output Low Voltage

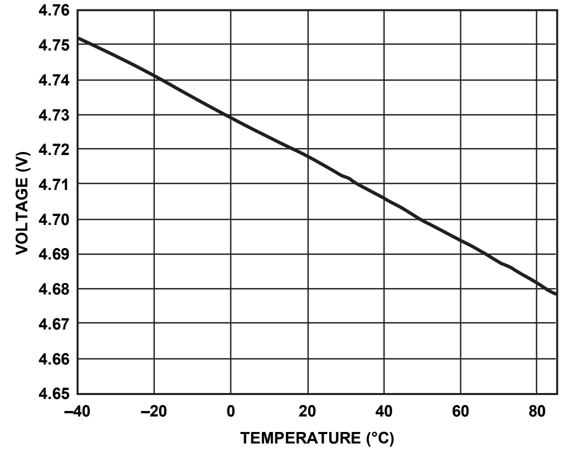

Figure 23. Receiver Output High Voltage vs. Temperature, $I_{RxD} = -4$ mA

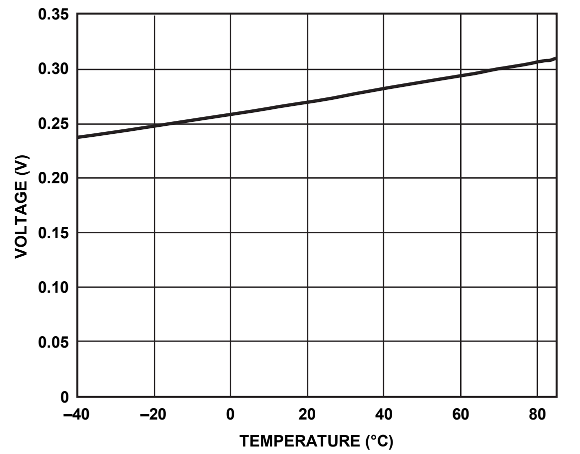

Figure 24. Receiver Output Low Voltage vs. Temperature, $I_{RxD} = -4$ mA

CIRCUIT DESCRIPTION

ELECTRICAL ISOLATION

In the ADM2491E, electrical isolation is implemented on the logic side of the interface. Therefore, the part has two main sections: a digital isolation section and a transceiver section (see Figure 25). The driver input signal, which is applied to the TxD pin and referenced to logic ground (GND_1), is coupled across an isolation barrier to appear at the transceiver section referenced to isolated ground (GND_2). Similarly, the receiver input, which is referenced to isolated ground in the transceiver section, is coupled across the isolation barrier to appear at the RxD pin referenced to logic ground.

iCoupler Technology

The digital signals are transmitted across the isolation barrier using *i*Coupler technology. This technique uses chip scale transformer windings to couple the digital signals magnetically from one side of the barrier to the other. Digital inputs are encoded into waveforms that are capable of exciting the primary transformer winding. At the secondary winding, the induced waveforms are decoded into the binary value that was originally transmitted.

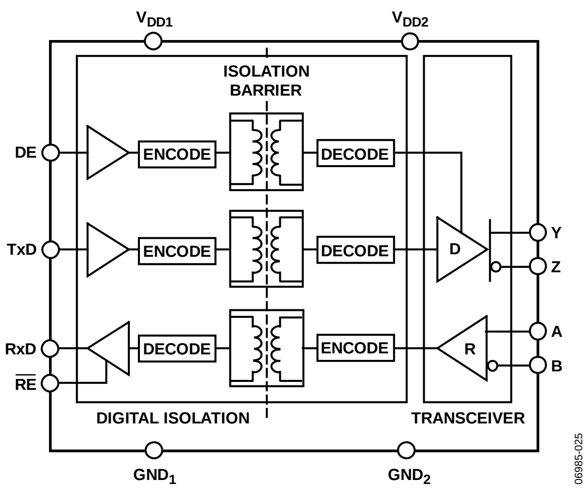

Figure 25. ADM2491E Digital Isolation and Transceiver Sections

TRUTH TABLES

The truth tables in this section use the abbreviations shown in Table 9.

Table 9. Truth Table Abbreviations

Letter	Description
H	High level
L	Low level
I	Indeterminate
X	Irrelevant
Z	High impedance (off)
NC	Disconnected

Table 10. Transmitting

Supply Status		Inputs		Outputs	
V_{DD1}	V_{DD2}	DE	TxD	Y	Z
On	On	H	H	H	L
On	On	H	L	L	H
On	On	L	X	Z	Z
On	Off	X	X	Z	Z
Off	On	L	L	Z	Z
Off	Off	X	X	Z	Z

Table 11. Receiving

Supply Status		Inputs		Output
V_{DD1}	V_{DD2}	A – B (V)	$\overline{RE}$	RxD
On	On	>0.2	L or NC	H
On	On	<−0.2	L or NC	L
On	On	−0.2 < A – B < +0.2	L or NC	I
On	On	Inputs open	L or NC	H
On	On	X	H	Z
On	Off	X	L or NC	H
Off	Off	X	L or NC	L

THERMAL SHUTDOWN

The ADM2491E contains thermal shutdown circuitry that protects the part from excessive power dissipation during fault conditions. Shorting the driver outputs to a low impedance source can result in high driver currents. The thermal sensing circuitry detects the increase in die temperature under this condition and disables the driver outputs. This circuitry is designed to disable the driver outputs when a die temperature of 150°C is reached. As the device cools, the drivers are re-enabled at a temperature of 140°C.

FAIL-SAFE RECEIVER INPUTS

The receiver inputs include a fail-safe feature that guarantees a logic high on the RxD pin when the A and B inputs are floating or open circuited.

MAGNETIC FIELD IMMUNITY

Because *i*Coupler devices use a coreless technology, no magnetic components are present and the problem of magnetic saturation of the core material does not exist. Therefore, *i*Coupler devices have essentially infinite dc field immunity. The following analysis defines the conditions under which this may occur. The 3 V operating condition of the ADM2491E is examined because it represents the most susceptible mode of operation.

The limitation on the ac magnetic field immunity of the *i*Coupler is set by the condition that induced an error voltage in the receiving coil (the bottom coil in this case) that was large to either falsely set or reset the decoder. The voltage induced across the bottom coil is given by

$$V = -\left(\frac{-d\beta}{dt}\right)\sum \pi r_n^{\,2}\ ;\ n = 1, 2, \ldots, N$$

where (if the pulses at the transformer output are greater than 1.0 V in amplitude):
β is the magnetic flux density (gauss).
N is the number of turns in the receiving coil.
r_n is the radius of the n^{th} turn in the receiving coil (cm).

The decoder has a sensing threshold of about 0.5 V; therefore, there is a 0.5 V margin in which induced voltages can be tolerated.

Given the geometry of the receiving coil and an imposed requirement that the induced voltage is, at most, 50% of the 0.5 V margin at the decoder, a maximum allowable magnetic field is calculated, as shown in Figure 26.

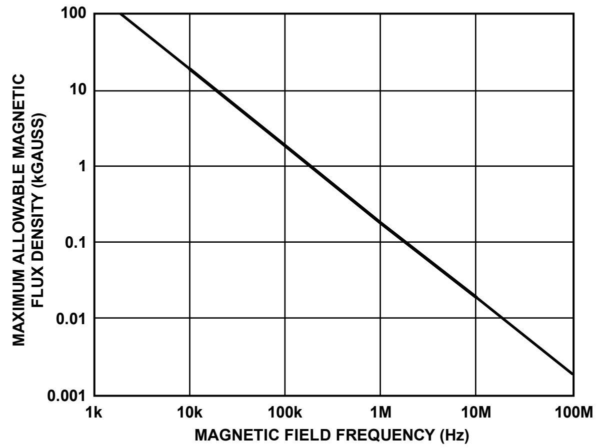

Figure 26. Maximum Allowable External Magnetic Flux Density

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.2 kgauss induces a voltage of 0.25 V at the receiving coil. This is about 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event occurs during a transmitted pulse and is the worst-case polarity, it reduces the received pulse from >1.0 V to 0.75 V—still well above the 0.5 V sensing threshold of the decoder.

Figure 27 shows the magnetic flux density values in terms of more familiar quantities, such as maximum allowable current flow, at given distances away from the ADM2491E transformers.

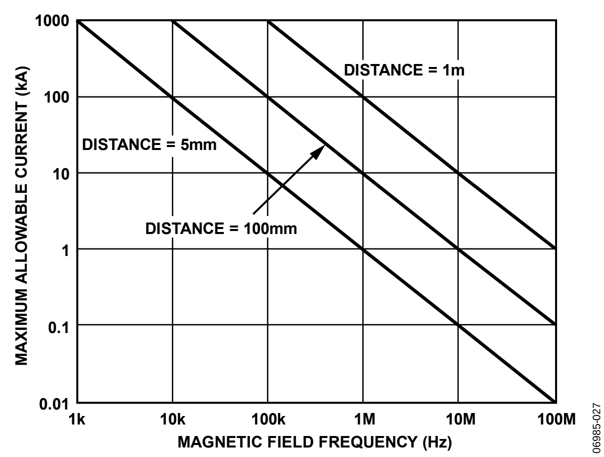

Figure 27. Maximum Allowable Current for Various Current-to-ADM2491E Spacings

With combinations of strong magnetic field and high frequency, any loops formed by printed circuit board traces can induce error voltages large enough to trigger the thresholds of succeeding circuitry. Care should be taken in the layout of such traces to avoid this possibility.

APPLICATIONS INFORMATION

ISOLATED POWER SUPPLY CIRCUIT

The ADM2491E requires isolated power capable of 5 V at up to approximately 75 mA (this current is dependent on the data rate and termination resistors used) to be supplied between the V_{DD2} and the GND_2 pins. A transformer driver circuit with a center-tapped transformer and LDO can be used to generate the isolated 5 V supply, as shown in Figure 28. The center-tapped transformer provides electrical isolation of the 5 V power supply. The primary winding of the transformer is excited with a pair of square waveforms that are 180° out of phase with each other. A pair of Schottky diodes and a smoothing capacitor are used to create a rectified signal from the secondary winding. The ADP3330 linear voltage regulator provides a regulated power supply to the bus-side circuitry (V_{DD2}) of the ADM2491E.

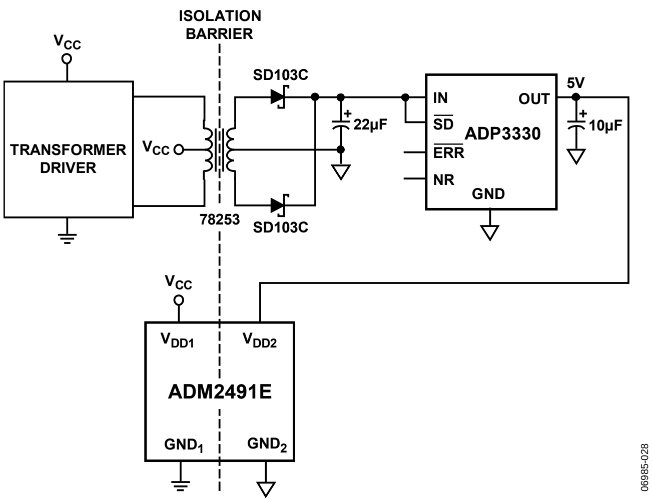

Figure 28. Isolated Power Supply Circuit

PCB LAYOUT

The ADM2491E isolated RS-485 transceiver requires no external interface circuitry for the logic interfaces. Power supply bypassing is required at the input and output supply pins (see Figure 29). Bypass capacitors are conveniently connected between Pin 1 and Pin 2 for V_{DD1} and between Pin 15 and Pin 16 for V_{DD2}. The capacitor value should be between 0.01 µF and 0.1 µF. The total lead length between both ends of the capacitor and the input power supply pin should not exceed 20 mm. Bypassing between Pin 1 and Pin 8 and between Pin 9 and Pin 16 should also be considered unless the ground pair on each package side is connected close to the package.

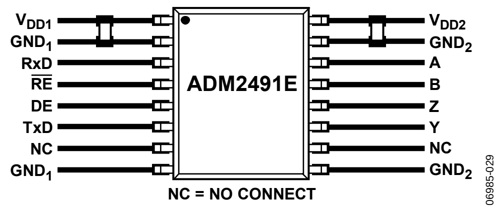

Figure 29. Recommended Printed Circuit Board Layout

In applications involving high common-mode transients, care should be taken to ensure that board coupling across the isolation barrier is minimized. Furthermore, the board layout should be designed such that any coupling that does occur equally affects all pins on a given component side. Failure to ensure this could cause voltage differentials between pins exceeding the absolute maximum ratings of the device, thereby leading to latch-up or permanent damage.

TYPICAL APPLICATIONS

Figure 30 and Figure 31 show typical applications of the ADM2491E in half-duplex and full-duplex RS-485 network configurations. Up to 32 transceivers can be connected to the RS-485 bus. To minimize reflections, the line must be terminated at the receiving end in its characteristic impedance, and stub lengths off the main line must be kept as short as possible. For half-duplex operation, this means that both ends of the line must be terminated because either end can be the receiving end.

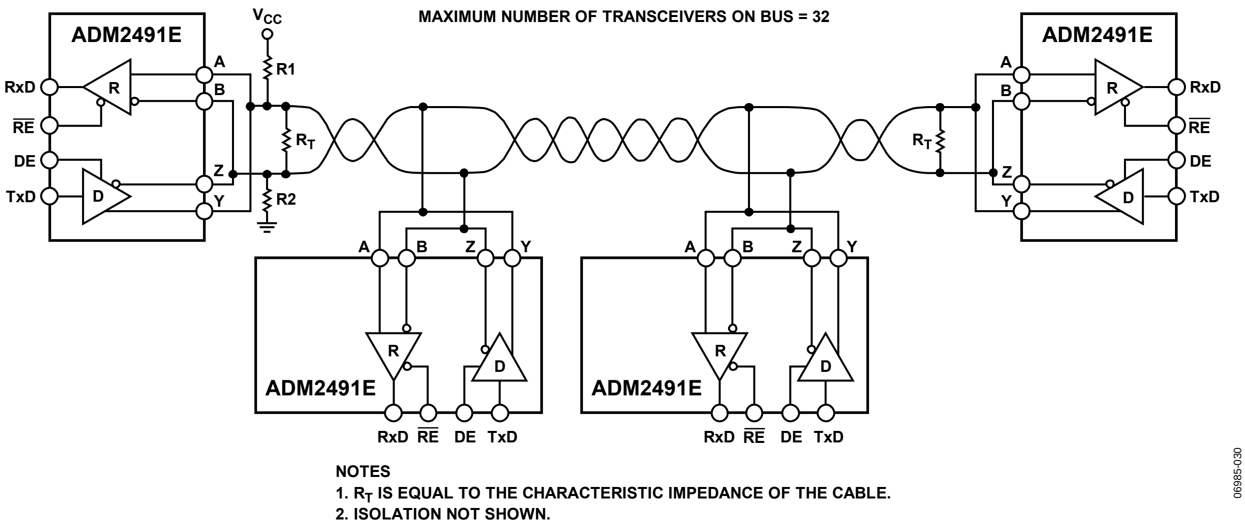

Figure 30. ADM2491E Typical Half-Duplex RS-485 Network

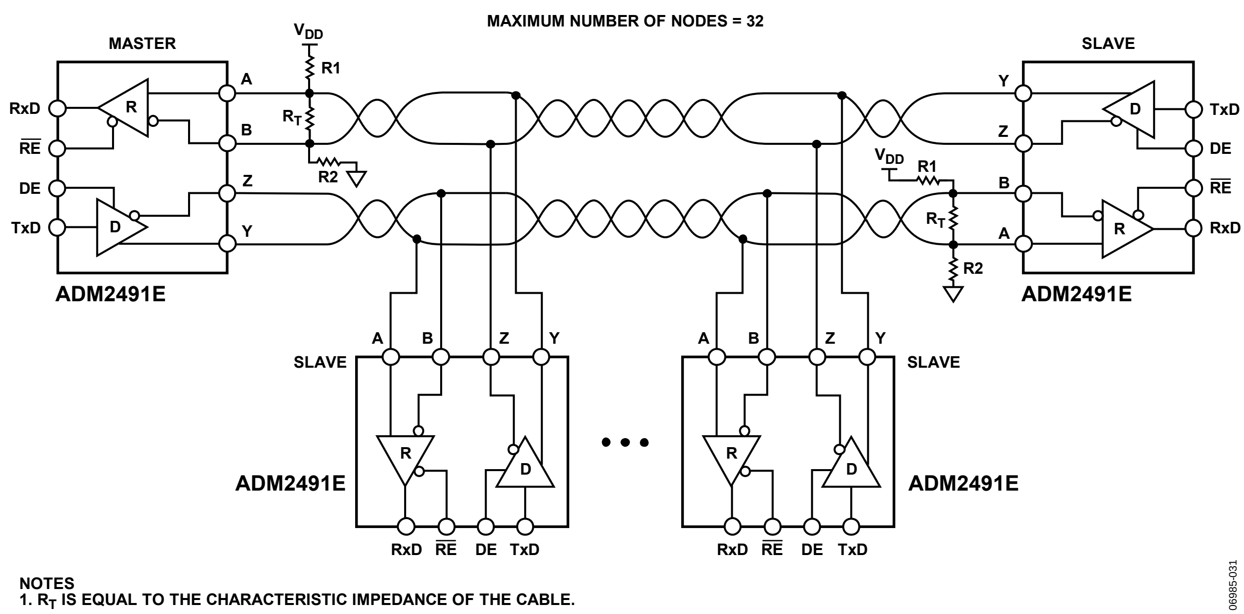

Figure 31. ADM2491E Typical Full -Duplex RS-485 Network

OUTLINE DIMENSIONS

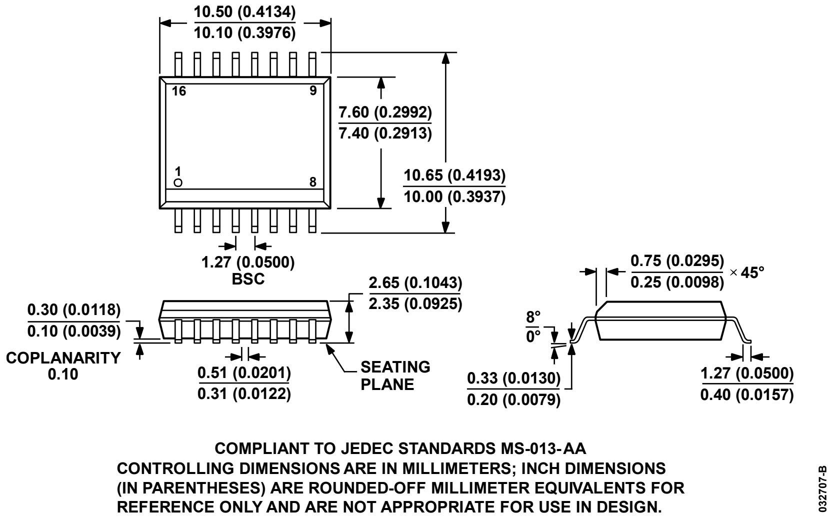

*Figure 32. 16-Lead Standard Small Outline Package [SOIC_W]
Wide Body
(RW-16)
Dimensions shown in millimeters and (inches)*

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADM2491EBRWZ[1]	−40°C to +85°C	16-Lead Standard Small Outline Package, Wide Body [SOIC_W]	RW-16
ADM2491EBRWZ–REEL7[1]	−40°C to +85°C	16-Lead Standard Small Outline Package, Wide Body [SOIC_W]	RW-16

[1] Z = RoHS Compliant Part.

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